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13. A switching circuit comprising:

at least one circuit for receiving a plurality of input clock signals delayed relative to one another and at least one control signal and outputting a new signal from among the plurality of input clock signals based upon the at least one control signal, the new signal being advanced or delayed relative to a current signal from among the plurality of input signals currently being output;

said at least one circuit outputting the new signal synchronously with a transition of the new signal and before disabling the current signal to substantially prevent the production of false signals during switching.

14. The switching circuit according to Claim 13 wherein said at least one circuit comprises a plurality of circuits each receiving a respective one of the plurality of input clock signals and selectively outputting its respective input clock signal as the new signal.

15. The switching circuit according to Claim 14 wherein said plurality of circuits are connected in a ring; and wherein each of said plurality of circuits provides a respective disabling signal upon being selected to adjacent circuits in the ring to disable said adjacent circuits.

16. The switching circuit according to Claim 15 further comprising a decoding circuit for decoding the at least one control signal, said decoding circuit providing at least one selection signal for activating one of said

plurality of circuits) based upon on a state of the at least one control signal.

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17. The switching circuit according to Claim 16 wherein each of the input clock signals is of equal period.

18. The switching circuit according to Claim 17 wherein each of the input clock signals is delayed equally relative to one another by a fraction equal to the period divided by a number of (said plurality of circuits).

19. The switching circuit according to Claim 16 wherein each disabling signal comprises a pulse; and wherein each of (said plurality of circuits) generates its respective pulse based upon the at least one selection signal.

20. The switching circuit according to Claim 19 wherein each of (said plurality of circuits) provides an enabling signal for enabling the transmission of its respective input clock signal based upon the at least one selection signal, the enabling signal being activated synchronously with a trailing edge of the respective input clock signal.

21. The switching circuit according to Claim 20 wherein each of (said plurality of circuits) deactivates its respective enabling signal upon receiving the disabling signal.

(22) A switching circuit comprising:

a plurality of circuits each receiving one of a plurality of input clock signals delayed relative to one another and a respective selection signal, one of said plurality of circuits selectively outputting its input clock signal as an output of the switching circuit based upon its selection signal;

each of said plurality of circuits selectively outputting its input clock signal synchronously with a transition of its input clock signal and before disabling a current output signal to substantially prevent the production of false signals during switching.

23. The switching circuit according to Claim 14 wherein said plurality of circuits are connected in a ring; and wherein each of said plurality of circuits provides a respective disabling signal to adjacent circuits in the ring upon being selected to disable said adjacent circuits.

24. The switching circuit according to Claim 22 wherein each of the input clock signals is of equal period.

25. The switching circuit according to Claim 24 wherein each of the input clock signals is delayed equally relative to one another by a fraction equal to the period divided by a number of said plurality of circuits.

26. The switching circuit according to Claim 23 wherein each disabling signal comprises a pulse; and wherein each of said plurality of circuits generates its respective pulse based upon its selection signal.

27. The switching circuit according to Claim 26 wherein each of said plurality of circuits provides an enabling signal for enabling the transmission of its input clock signal based upon its selection signal, the enabling signal being activated synchronously with a trailing edge of the respective input clock signal.

28. The switching circuit according to Claim 27 wherein each of said plurality of circuits deactivates its respective enabling signal upon receiving the disabling signal.

29. A circuit for recovering data from a serial data flow comprising:

a generator for generating a plurality of clock signals of equal period that are delayed equally relative to one another by a fraction equal to the period divided by a number of the plurality of clock signals;

a switching circuit for receiving the plurality of clock signals and providing one of the clock signals as an output thereof;

a phase comparator for receiving the output from said switching circuit and a data flow signal comprising a flow of data and providing at least one phase difference signal indicating a phase difference therebetween; and

a controller for receiving the at least one phase difference signal from said phase comparator and controlling the switching circuit based thereon to switch the output of said switching circuit to one of said clock signals providing a smaller phase difference than a current clock signal;

said switching circuit providing the output synchronously with a transition of the output and before disabling a current output to substantially prevent the production of false signals during switching.

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30. The circuit according to Claim 29 wherein said generator comprises a delay-locked loop circuit.

31. The circuit according to Claim 29 further comprising a data sampler receiving as inputs the data flow signal and the output of said switching circuit; and wherein the output of said switching circuit synchronizes sampling of the data flow signal by said data sampler.

32. A method for switching between a plurality of input clock signals delayed relative to one another comprising:

selecting a new signal from among the plurality of input clock signals based upon at least one control signal, the new signal being advanced or delayed relative to a current signal of the plurality of input signals currently selected; and

outputting the new signal synchronously with a transition of the new signal and before disabling the current signal to substantially prevent the production of false signals during switching.

33. The method according to Claim 32 wherein each of the input clock signals is of equal period.